What is claimed is:

1. A semiconductor device, comprising:

memory cells each having an area of about $6F^2$;

sense amplifiers;

bit lines coupled to the sense amplifiers in a folded bit line configuration, each bit line including a first level portion and a second level portion; and

active area lines, transistors being formed in the active area lines and electrically coupling corresponding memory cells to corresponding first level bit lines.

2. The semiconductor device of claim 1, wherein each pair of bit lines is vertically twisted at one or more predetermined locations, the bit lines in the pair transitioning between the first level portion and the second level portion at each twist.

3. The semiconductor device of claim 2, wherein a column pitch of each memory cell is 2F.

4. The semiconductor device of claim 1, wherein each memory cell includes a capacitor formed over the first level portion of each bit line.

5. The semiconductor device of claim 4, wherein the second level portion of each bit line is formed over each capacitor.

6. The semiconductor device of claim 1, wherein the bit lines extend generally along the same direction as the active area lines, the bit lines intersecting the active area lines at slanted portions,

the semiconductor device further comprising contacts between the bit lines and active area lines formed in the slanted portions.

7. The semiconductor device of claim 6, wherein the active area lines are generally straight and the bit lines extend in a wavy pattern.

8. The semiconductor device of claim 6, wherein the bit lines are generally straight and the active area lines extend in a wavy pattern.

9. The semiconductor device of claim 6, each bit line having a first portion on a first side of a corresponding active area line, a second portion on a second side of the corresponding active area line, and a third portion on the first side of the active area line.

10. The semiconductor device of claim 6, wherein the bit lines extend along generally the same direction as the active area lines so that the bit lines and active area lines intersect at predetermined locations.

11. A memory device comprising:

memory cells each having an area of about $6F^2$;

sense amplifiers;

bit lines coupled to the sense amplifiers in a folded bit line arrangement;

active area lines; and

transistors formed in the active area lines and electrically coupling corresponding memory cells to corresponding bit lines.

12. The memory device of claim 11, wherein each bit line has a first level portion and a second level portion, each transistor electrically coupling a corresponding memory cell to a first level portion of a corresponding bit line.

13. The memory device of claim 12, wherein each pair of bit lines is vertically twisted at one or more predetermined locations, the bit lines in the pair transitioning between the first level portion and the second level portion at each twist.

14. The memory device of claim 12, wherein each memory cell includes a capacitor formed over the first level portion of each bit line.

15. The memory device of claim 14, wherein the second level portion of each bit line is formed over each capacitor.

16. The memory device of claim 11, wherein the bit lines extend generally along the same direction as the active area lines, the bit lines intersecting the active area lines at slanted portions.

17. The memory device of claim 11, wherein each pair of bit lines is coupled to one side of a corresponding sense amplifier.

18. A method of making a memory device, comprising:

forming memory cells each having an area of about $6F^2$;

forming sense amplifiers;

coupling bit lines to the sense amplifiers in a folded bit line arrangement;

forming transistors in active area lines; and

the transistors electrically coupling corresponding memory cells to corresponding bit lines.

19. The method of claim 18, further comprising:

forming each bit line of a first level portion and a second level portion; and

coupling each transistor to the first level portion of the corresponding bit line.

20. The method of claim 19, further comprising:

vertically twisting each pair of bit lines at one or more predetermined locations; and

transitioning the bit lines in the pair between the first level portion and the second level portion at each twist.

21. The method of claim 20, further comprising forming a capacitor of each memory cell over the first level portion of each bit line.

22. The method of claim 21, further comprising forming the second level portion of each bit line over the capacitor.